LISTING OF THE CLAIMS

1. (original) A capacitor comprising:

a substrate;

a first capacitor plate layer formed over the substrate, the first capacitor plate layer comprising a horizontally separated and interconnected first series of tines;

a second capacitor plate layer separated from the first capacitor plate layer by a capacitor dielectric layer, the second capacitor plate layer comprising a horizontally separated and interconnected second series of tines horizontally interdigitated between the horizontally separated and interconnected first series of tines, wherein the capacitor dielectric layer is a single serpentine conformal dielectric layer sequentially:

formed upon a top surface of a first tine;

formed interposed between a first tine and a second tine;

formed beneath a bottom surface of a second tine; and

formed interposed between the second tine and an additional first tine.

2. (original) The capacitor of claim 1 wherein the second series of tines is horizontally interdigitated but not vertically interdigitated with respect to the first series of tines.

3. (original) The capacitor of claim 1 wherein the substrate is a semiconductor substrate.

4. (original) The capacitor of claim 1 wherein the substrate is a ceramic substrate.

5. (original) The capacitor of claim 1 wherein the capacitor dielectric layer is formed to a thickness of from about 20 to about 200 angstroms.

6. (original) The capacitor of claim 1 wherein the second capacitor plate also covers a series of top surfaces of the first series of tines.

7. (withdrawn) A method for fabricating a capacitor comprising:

providing a substrate;

forming a first capacitor plate layer over the substrate, the first capacitor plate layer comprising a horizontally separated and interconnected first series of tines that defines a series of apertures;

forming a conformal capacitor dielectric layer upon the patterned first capacitor plate layer, the conformal capacitor dielectric layer not completely filling the series of apertures; and

forming a second capacitor plate layer upon the capacitor dielectric layer and completely filling the series of apertures to form a horizontally separated and interconnected second series of tines horizontally interdigitated between the horizontally separated and interconnected first series of tines.

8. (withdrawn)The method of claim 7 wherein the substrate is a semiconductor substrate.

9. (withdrawn) The method of claim 7 wherein the series of apertures is formed of a minimum photolithographically resolvable aperture width.

10. (withdrawn) The method of claim 7 wherein the conformal capacitor dielectric layer is formed to a thickness of from about 20 to about 200 angstroms.

11. (withdrawn) The method of claim 7 wherein the second series of tines is formed self-aligned with respect to the first series of tines.

12. (withdrawn) The method of claim 7 wherein the second series of tines is formed horizontally interdigitated but not vertically interdigitated with respect to the first series of tines.

13. (withdrawn) The capacitor of claim 7 wherein the second capacitor plate also covers a series of top surfaces of the first series of tines.

14. (withdrawn) A method for fabricating a capacitor comprising:

providing a substrate;

forming a first capacitor plate layer over the substrate, the first capacitor plate layer comprising a horizontally separated and interconnected first series of tines that defines a series of apertures;

forming a conformal capacitor dielectric layer upon the patterned first capacitor plate layer, the conformal capacitor dielectric layer not completely filling the series of apertures;

forming a second capacitor plate layer upon the capacitor dielectric layer and completely filling the series of apertures to form a horizontally separated and interconnected second series of tines horizontally interdigitated between the horizontally separated and interconnected first series of tines; and

planarizing the second capacitor plate layer.

15. (withdrawn) The method of claim 14 wherein the substrate is a semiconductor substrate.

16. (withdrawn) The method of claim 14 wherein the series of apertures is formed of a minimum photolithographically resolvable aperture width.

17. (withdrawn) The method of claim 14 wherein the conformal capacitor dielectric layer is formed to a thickness of from about 20 to about 200 angstroms.

18. (withdrawn) The method of claim 14 wherein the second series of tines is formed self-aligned with respect to the first series of tines.

19. (withdrawn) The method of claim 14 wherein the second series of tines is formed horizontally interdigitated but not vertically interdigitated with respect to the first series of tines.

20. (withdrawn) The capacitor of claim 14 wherein the second capacitor plate also covers a series of top surfaces of the first series of tines.